OIPE JC34
AUG 2 4 2001
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Mahalingam Nandakumar, et al. Art Unit: 2811

Serial No.: 09/876,292 Examiner: TBD

Filed: 06/07/01 Docket: TI-31089

For: Additional n-Type LDD/Pocket Implant for Improving Short-Channel NMOS ESD Robustness

#4

LETTER TO THE OFFICIAL DRAFTSPERSON

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service on 8-20-01 as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents Application Processing Division's Customer Correction Branch, Washington, D.C. 20231.

Karen Vertz 8-20-01
Karen Vertz Date

Assistant Commissioner for
Patents
Washington, D. C. 20231

Dear Sir:

Enclosed are **FOUR (4)** sheets of formal drawings for the above-referenced case. Please charge any necessary fees to Deposit Account No. 20-0668 of Texas Instruments Incorporated. This sheet is enclosed in triplicate.

Respectfully submitted,

Gary C. Honeycutt

Texas Instruments Incorporated
P.O. Box 655474 M/S 3999
Dallas, Texas 75265
(972) 238-7160

Gary C. Honeycutt
Reg. No. 20,250
Attorney for Applicants